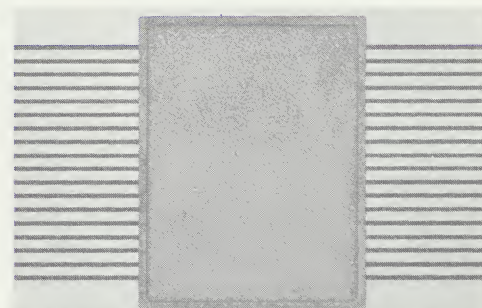
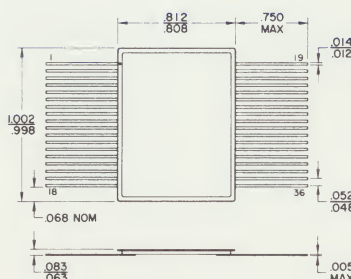
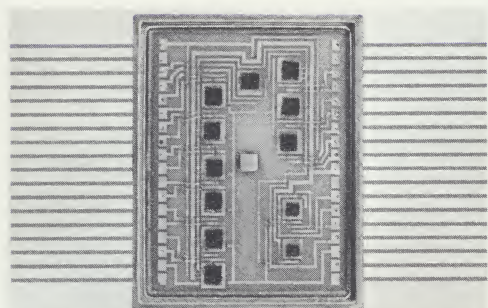


AMELCO

SHIFT REGISTER

5551 BM

5552 BM



These devices consist of dual binary elements interconnected to form a 16 or 20 bit shift register and packed in a MEMA (Micro-Electronic Modular Assembly). The registers are designed for serial or parallel operation.

ELECTRICAL CHARACTERISTICS 25°C

Supply Voltage	+7 volts	pin 6	Clock Input	
	+5 volts	pin 36		V_{in} High 1.8 volts
	Ground	pin 9		V_{in} Low 1.0 volts
Power Dissipation	190 mw	(20 bit-5551 BM)		I_{in} high 20 μ A at 3.0 volts
	160 mw	(16 bit-5552 BM)		I_{in} low 800 μ A
Data Input			Data Output	
	V_{in} High	1.8 volts		V_{out} High 2.5 volts
	V_{in} Low	1.0 volts		V_{out} Low 300 mV at 1.5 mA
	I_{in} high	3.0 μ A at 3.0 volts		Minimum Pulse Width 200 n Sec
	I_{in} low	600 μ A		Maximum Clock Rate 1 mc

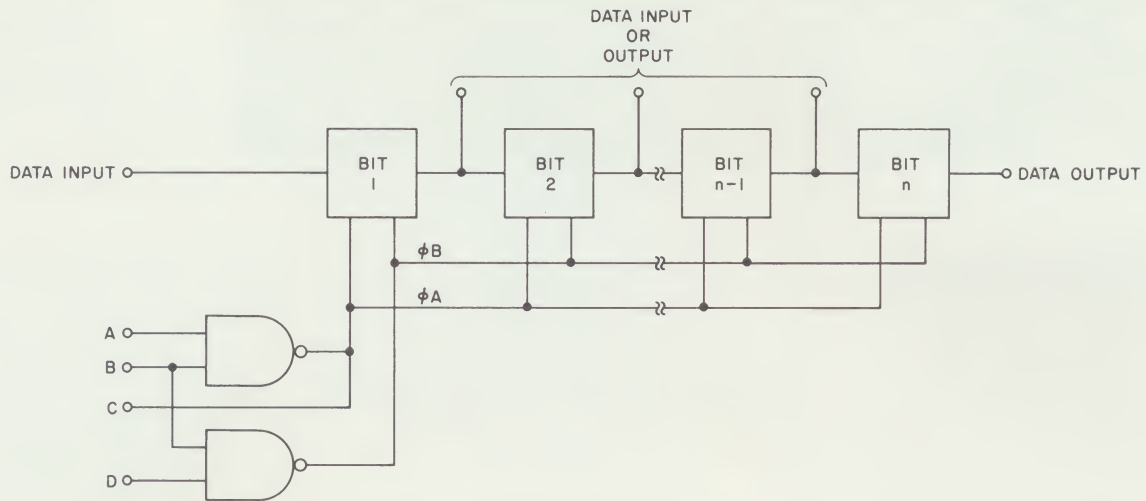
AMELCO SEMICONDUCTOR

DIVISION OF TELEDYNE, INC./1300 TERRA BELLA AVENUE, MOUNTAIN VIEW, CALIFORNIA

Mail Address: P. O. Box 1030, Mountain View, California • Telephone (415) 968-9241 • TWX: (415) 969-9112



BLOCK DIAGRAM



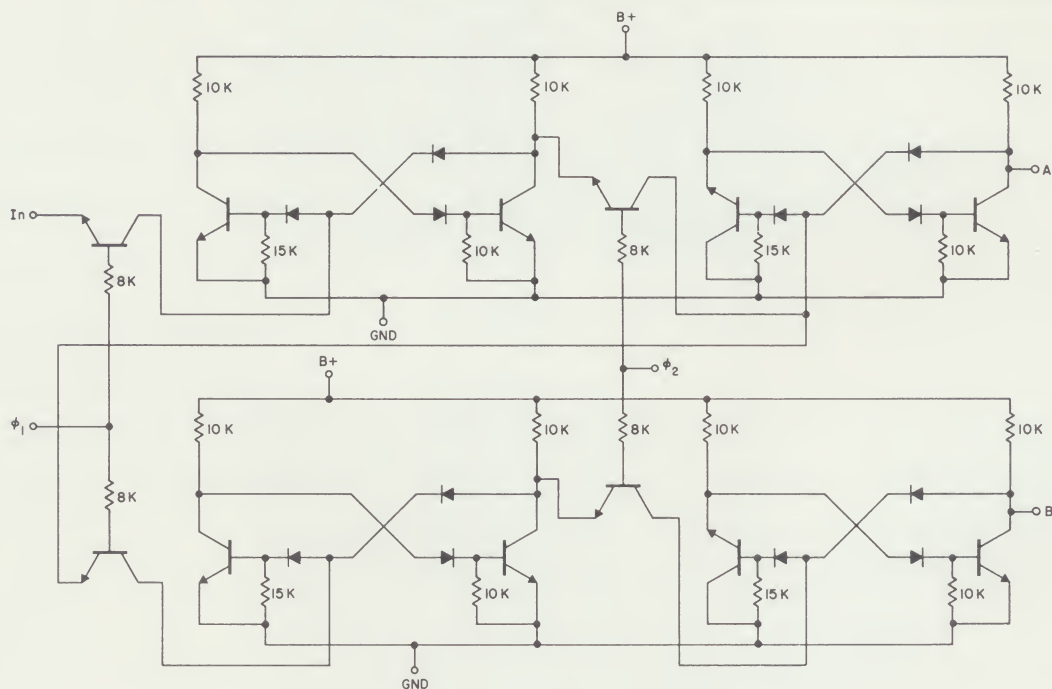
Single Phase Operation: Input at A is ϕA and tie C to D.

Two Phase Operation: Input at A is $\overline{\phi A}$ and input at D is $\overline{\phi B}$.

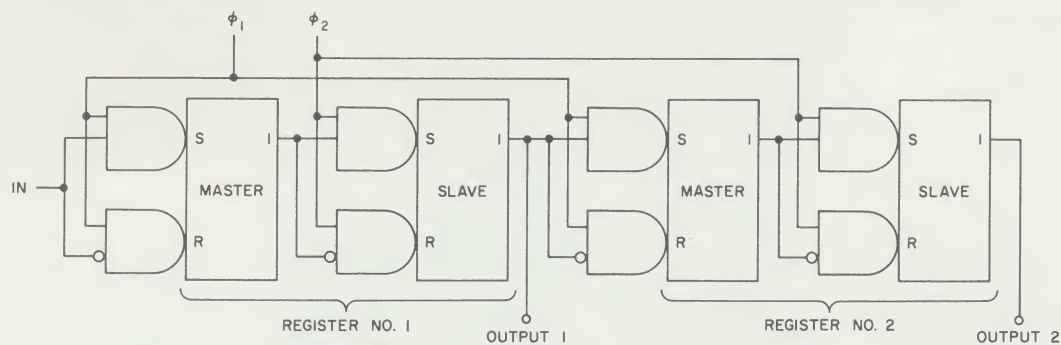
Data shift occurs when ϕA is low and ϕB is high.

Register will be reset by propagating state of Bit 1 through register when ϕA and ϕB are high. Reset time is less than 200 nsec.

ELECTRICAL SCHEMATIC



LOGIC DIAGRAM



PIN CONNECTIONS

5551

20 BIT REGISTER (Note 1)

Data Input
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)
Data Output (or Input)

$\phi\bar{A}$ Clock Input

External Gate Input

ϕA Clock

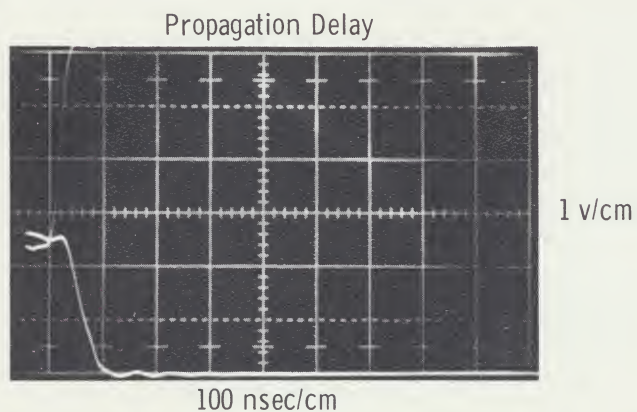
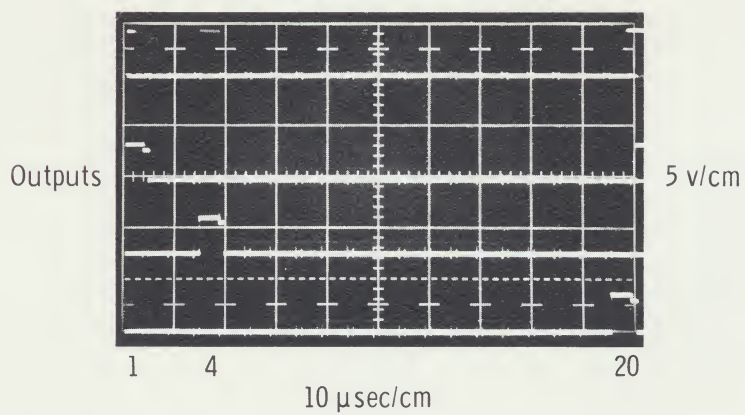
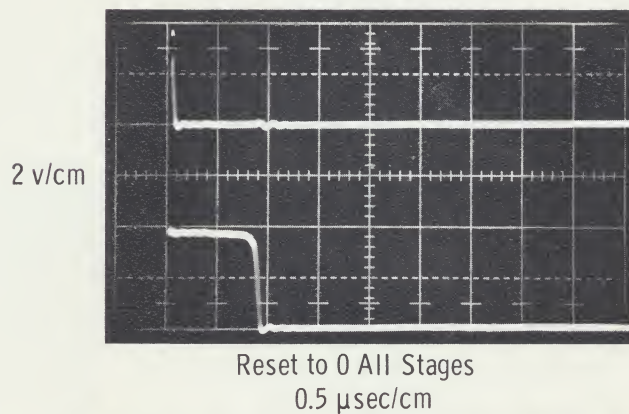
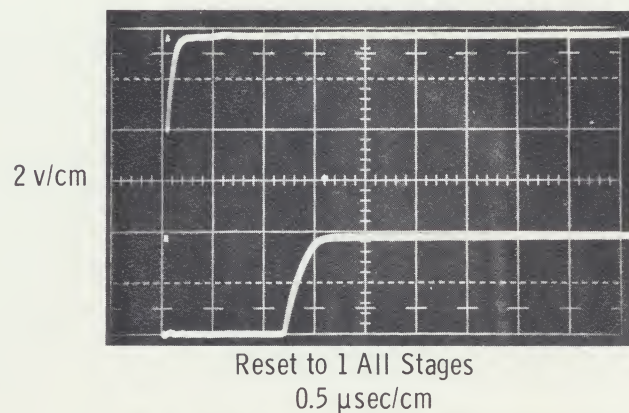
$\phi\bar{B}$ Clock Input

Bit 1	Pin 11
Bit 1	Pin 12
Bit 2	Pin 13
Bit 3	Pin 14
Bit 4	Pin 15
Bit 5	Pin 16
Bit 6	Pin 34
Bit 7	Pin 33
Bit 8	Pin 32
Bit 9	Pin 31
Bit 10	Pin 30
Bit 11	Pin 29
Bit 12	Pin 28
Bit 13	Pin 27
Bit 14	Pin 26
Bit 15	Pin 25
Bit 16	Pin 24
Bit 17	Pin 23
Bit 18	Pin 22
Bit 19	Pin 21
Bit 20	Pin 20
A	Pin 4
B	Pin 5
C	Pin 3
D	Pin 7

(Note 1) 5552 — 16 Bit Register does not use pins 20, 21, 22, 23

TIMING DIAGRAMS

Time to Reset 20 Bit Shift Register



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